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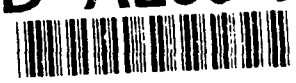

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13. ABSTRACT *(Maximum 200 words)*

The following document details the results of efforts to develop a high temperature sensor technology based in Kopin's proprietary ISE^{tm} SOI material. Results are presented from a detailed analysis of the piezoresistive properties, and of the internal stress in the layer. These results show the material to be electrically similar to bulk, with very low internal stress. This makes ISE^{tm} an ideal material choice for this application.

A full sensor process sequence, with mask set, and enabling process equipment and techniques, was developed for this program. In parallel with the process development, extensive circuit analysis and modeling was performed to identify the best high temperature sensing circuit for this task. After modeling, test circuits were fabricated in bulk wafers to evaluate the design. The final design, a switching capacitive MOS circuit with proportional output, is expected to produce a sensor with 0.1% accuracy over the temperature range of -60°C to 300°C. Kopin is currently pursuing industrial financing for Phase III of this work to complete the integration of this work for commercial application.

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SMART MICROSENSORS

FOR

HIGH TEMPERATURE APPLICATIONS

FINAL REPORT

by D. P. Vu, M. W. Batty, J. C. C. Fan

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I) INTRODUCTION

This document represents the final report on a program to develop physical sensors in SOI material. A primary motivation of this activity was the development of devices with a capability to operate at high temperatures. During the initial stages of the program, a decision was made to focus attention on a pressure sensors. Several technical issues had to be addressed. The Piezoresistive properties of ISE^{tm} films had not previously been characterized, nor had measurements of film stress been examined. These measurements were carefully conducted and the results are reported within this document. Simultaneously with these evaluations, Kopin proceeded to develop a mask set which contained a number of pressure sensing elements of various sizes. The mask set contains both capacitive and Piezoresistive pressure sensors and a simple accelerometer. A process was developed which produced single crystalline silicon diaphragms supported by polysilicon.

Operation at elevated temperature is a primary goal of this work. Prior to the start of the program, the high temperature performance of ISE^{tm} CMOS circuits had been demonstrated. Bipolar circuits in ISE^{tm} material have not been as successfully implemented and a decision was made to pursue MOS analog circuit design in SOI. After several iterations it became apparent that the preferred sensor would be a capacitive type coupled to an MOS switching circuit. Extensive analysis of circuit designs was conducted. In many of the designs evaluated, an operational amplifier was required. We designed and built test circuits in bulk silicon for evaluation. Our final circuit choice is a switching capacitor circuit whose output is proportional to the difference between a reference and measured capacitor. This implementation should provide a 0.1% pressure measurement over a temperature range extending from -60°C to 300°C.

While a completely integrated device has not yet been fabricated, Kopin has made significant progress in achieved this goal. Results from this work have substantiated our opinion that ISE^{tm} material will provide sensors with superior performance. Kopin is pursuing industrial financing for the Phase III program. We have attended a meeting held in Boston by SEMA and presented our results. The reception was warm and several contacts were provided. We are currently pursuing these leads. In addition, Kopin has contacted a large US sensor manufacturer who has interest in applying silicon sensors to industrial process control.

II) TECHNICAL ACHIEVEMENTS DURING THIS PROGRAM:

2.1) Task 1: Diaphragm Design

At the completion of the Phase I program, Kopin had demonstrated single crystal silicon diaphragms fabricated using its Zone-Melting-Recrystallization (ZMR) process. Diaphragms were created by patterning the oxide on the starting wafer prior to the ZMR process. Polysilicon was then deposited and the wafers were capped with a deposited oxide. The polysilicon was converted to single crystalline silicon in Kopin's ISE^{tm} machines. Subsequent processing freed the diaphragms from the substrates to complete the device. While this process worked, the thickness non- uniformity of the resultant diaphragm was nearly 50%, an unacceptable value for acceptable sensors.

As a result, Kopin proceeded to develop a process that used finished ISE^{tm} wafers as the starting material. This procedure had two main advantages, the first being that the diaphragm uniformity would be that of the starting ISE^{tm} wafer or about ±2%, and that sensors could be fabricated by other manufacturers without the need to establish an ISE^{tm} capability in-house. A mask set was developed and the new process was tested successfully, demonstrating 600μm square diaphragms.

2.2) Task 2: Circuit Design

The goal of this program was to achieve high temperature smart microsensors using SOI materials as their foundation. In concert with these objectives we decided to focus our circuit development efforts on capacitive measuring circuits. This decision is based on the temperature coefficient of the piezoresistors and the apparent circuit complexity required to overcome these temperature effects. Capacitors have essentially no temperature coefficient and are compatible with the objectives of the program. Evaluation of circuit designs revealed that very simple MOS analog circuits can be employed as is reported in the body of this text.

The fundamental circuit elements needed to complete a switching capacitor measurement circuit include analog switches and operational amplifiers. During this program, we designed an MOS operational amplifier and tested the design on bulk silicon wafers. Kopin plans to fabricate the entire circuit in SOI and test its performance at temperature. Insufficient time was available to complete this task during this contract.

2.3) Task 3: Fabrication

As indicated above, diaphragms were successfully fabricated in ISE^{tm} wafers. During the development of the pressure sensor, Kopin invented a technique for freeing the diaphragms from the substrate and avoiding an adhesion problem that plagued our initial efforts. Among the several approaches explored by Kopin, effort was concentrated on "freeze-drying", vapor phase HF etching and alcohol displacement and vaporization. While all three techniques worked, the latter was the simplest and most effective.

Surface micromachining techniques were developed to create free standing silicon diaphragms in SOI wafers. An initial process and mask set was established yielding encouraging results. Problems with dimensional control during etching steps required modifications to the mask set. The revised mask set yielded fully supported diaphragms.

2.4) Task 4: Measurements

Measurements were conducted on the mechanical properties of the SOI material. A mask set was created for the purpose of determining the stress in the SOI films. We have found that there is a slight orientation dependence but that the stress levels are extremely low. Our current estimates suggests a slightly tensile material with a stress level below 10^8 dynes/cm^2. These excellent results support our believe that ISE^{tm} SOI will produce superior low pressure sensors.

Under this task, Kopin characterized the piezoresistive properties of the thin silicon layer. This was of extreme importance to the program since results on polysilicon showed performance significantly poorer than bulk silicon. Based on our results, we found that ISE^{tm} wafers have the same Piezoresistive characteristics as bulk silicon.

2.5) Task 5: Modeling

SPICE modeling of the circuit design has been conducted and is reported in the body of this report. These results indicated that the circuit will perform as expected.

III) MATERIAL ANALYSIS

3.1) Piezoresistive Properties

In this section, we report our results measuring the piezoresistance of SOI films produced using the Kopin's ISE^{tm} process. These results are compared with published data on the piezoresistance of poly silicon, laser recrystallized silicon and bulk silicon. It has been determined that piezoresistors fabricated in ISE^{tm} are equivalent to bulk resistors.

3.1.1) Wafer Preparation

Wafers were prepared at Kopin Corporation using their proprietary ISE^{tm} process. This process is a refinement of the ZMR process. In the ISE^{tm} process, a bulk silicon wafer is prepared by first growing a thermal oxide, followed by deposition of a thin polycrystalline silicon film, and finally by capping the structure with a CVD oxide (see Figure 1). The wafer is then placed in a system which consists of a lower substrate platen/heater, and an upper wire heater as shown in Figure 2. The substrate temperature is raised to about 1200°C, and the upper wire is heated and scanned such that only the thin silicon film at the surface of the wafer melts and recrystallizes. Subsequently the capping layer is removed and the SOI formation is complete.

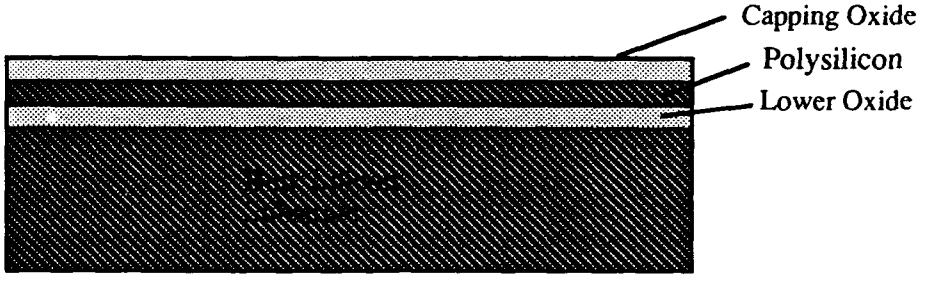


Figure 1. Cross-section of a starting ISE^{tm} wafer.

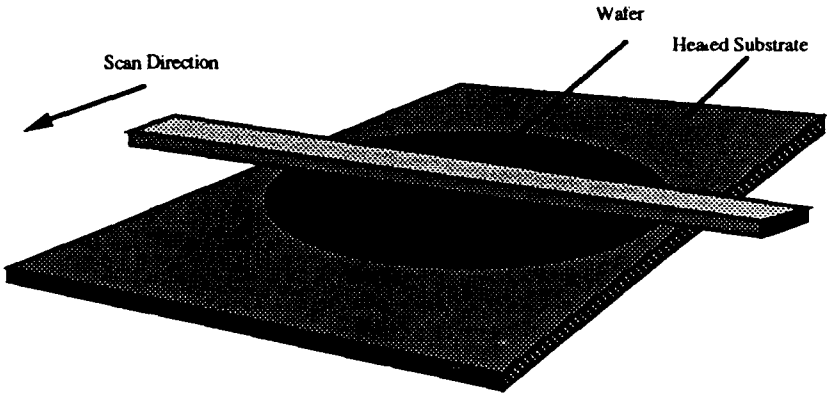


Figure 2. Schematic representation of the ISE^{tm} process.

ISE^{tm} wafers can only be obtained with epitaxial layers oriented in the (100) direction. For this program, one micron silicon films on one micron of silicon dioxide were fabricated on (100) oriented 10ohm-cm phosphorous doped substrates. The background density of the initial thin silicon epitaxial layer is less than $10^{15}/cm^3$. This material was doped with boron at four different levels in a range between $10^{17}/cm^3$ and $10^{19}/cm^3$. After doping, the samples were patterned and etched to define the single crystalline silicon piezoresistors. These were oxidized at 1100°C in dry O_2 and annealed in N_2 for a sufficient time to produce a uniform dopant density. Contact openings were cut into the oxide and aluminum was deposited and annealed to yield the complete test structures.

3.1.2) Measurement Conditions

ISE^{tm} wafers were prepared with a range of dopant densities from $1x10^{17}/cm^2$ to $1x10^{19}/cm^2$. Each wafer was processed to create five samples each about 0.5" wide and about 1.5" long as shown in figure 3. The sample would ultimately be clamped at its mid point so that one end of the beam could be deflected. The clamping point was defined by two markers as shown in the figure. The six piezoresistors to be measured were patterned near the clamp on the side undergoing deflection in pairs of three orientations; longitudinal, diagonal and transverse. The resistors share a common electrical return. Two additional resistors at the unstressed end of the beam near the contact pads were defined and used as controls during the measurement. In addition, a four point resistivity structure and a metal contact resistance structure were included as a check on our process.

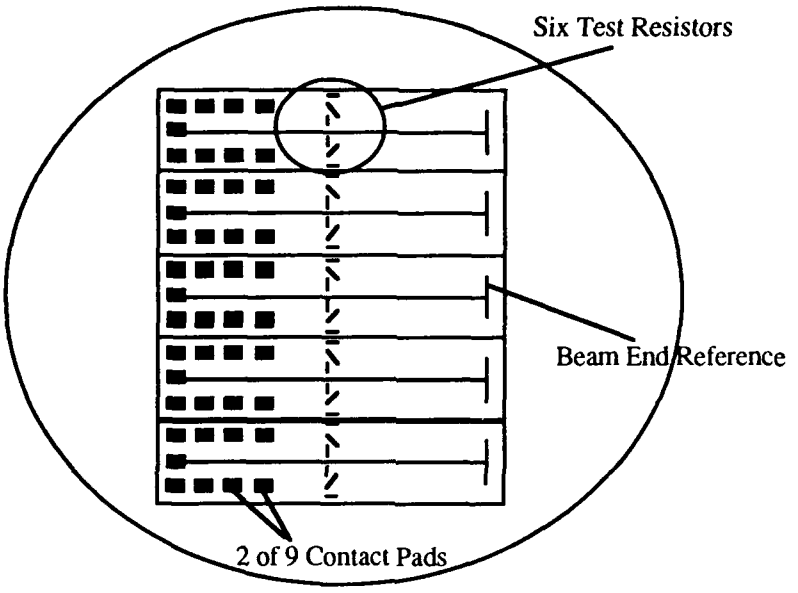


Figure 3. Layout of a wafer with 5 piezoresistance test chips.

After the wafers were processed and diced, a single sample was loaded into a simple holder for testing. The holder consisted of a clamp and probe assembly, a plunger and a proximity probe as shown in figure 4. The clamp and probe assemble had an channeled aluminum base into which the sample could be loaded and positioned. A second spring loaded Teflon rocker arm was used to both clamp the sample and support the nine probes needed to contact the six test resistors, the two control resistors and the common electrical return. Gold plated pogopins were used to make contact to the aluminum contact pads on the sample. Consistent reproducible contacts were made to the sample in this manner.

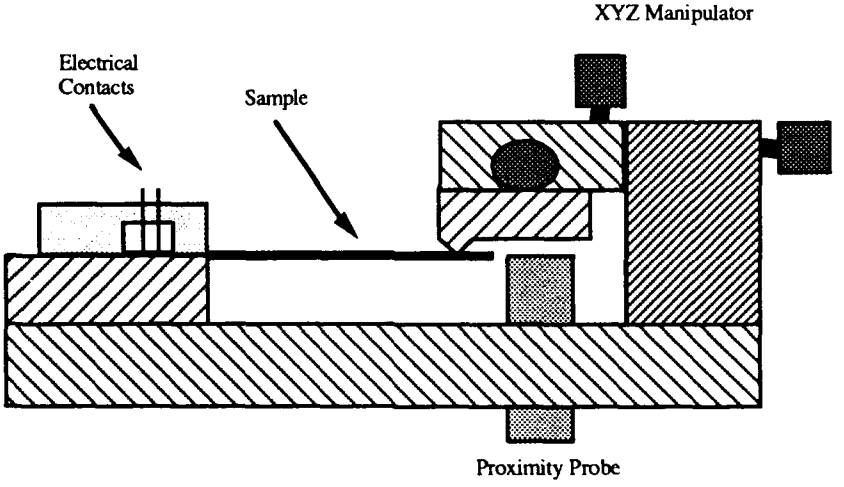


Figure 4. Test set-up for piezoresistance measurement.

An xyz manipulator supported a plunger near the end of the beam. Its position in the z-direction was measured using a capacitive proximity probe. The flat square edge of the plunger was adjusted such that it contacted the sample at the point indicated at the end of the beam. In this way, the deflection and therefore strain in the beam was well controlled. During a measurement the strain was varied between 0 and 0.001.

Measurements were made inside an oven whose temperature adjusted in the range between about 25°C and 150°C. Two terminal resistance measurements were made on all eight resistors at twenty strain levels. In addition, the resistance of the unstrained sample before and after the measurement were recorded.

3.1.3) Data Reduction

Data collected on the samples were loaded into a spreadsheet for analysis. Due to variations in the oven temperature during the measurement, sample resistance would vary. The control resistors were incorporated to help account for this variation. The temperature indicated for the oven was recorded at the beginning of the measurement. The value of the two control resistors at each stress point was then compared with the first unstressed measurement and the $\Delta R/R$ calculated for each point. The average $\Delta R/R$ of the two control resistors would then be used to adjust the measured value of the other six test resistors.

The position measurement described above was made on the plunger and not the sample. Therefore, only changes in deflection were measured and the absolute value of the beam deflection was not known. As a check on the integrity of the data, the average value of the temperature compensated data was used to determine the zero position. In general the zero value predicted using this technique was in good agreement among the transverse and longitudinal resistors but was in poor agreement for the diagonal resistors. The poor result on the diagonal resistors is a direct result of their low sensitivity to strain.

Gage factors for the resistors were calculated on the temperature compensated data. The strain (ε) in the beam was calculated using

$$\varepsilon(\partial) = 3/2t * (1-x) * \partial/l^3$$

where

t is the beam thickness,

x is the counter point of the resistors relative to the clamp,

∂ is the deflection.

Since the strain varies linearly along the beam, the strain calculated above will be the average strain experience by the piezoresistor.

In figure 5 we show a typical plot of the raw data collect. along with a line representing a least squares fit to the data. The slope of the line is proportional to the gage factor (G) through

$$G = \text{slope}/a,$$

where

$$a = 3/2t * (1-x)/l^3.$$

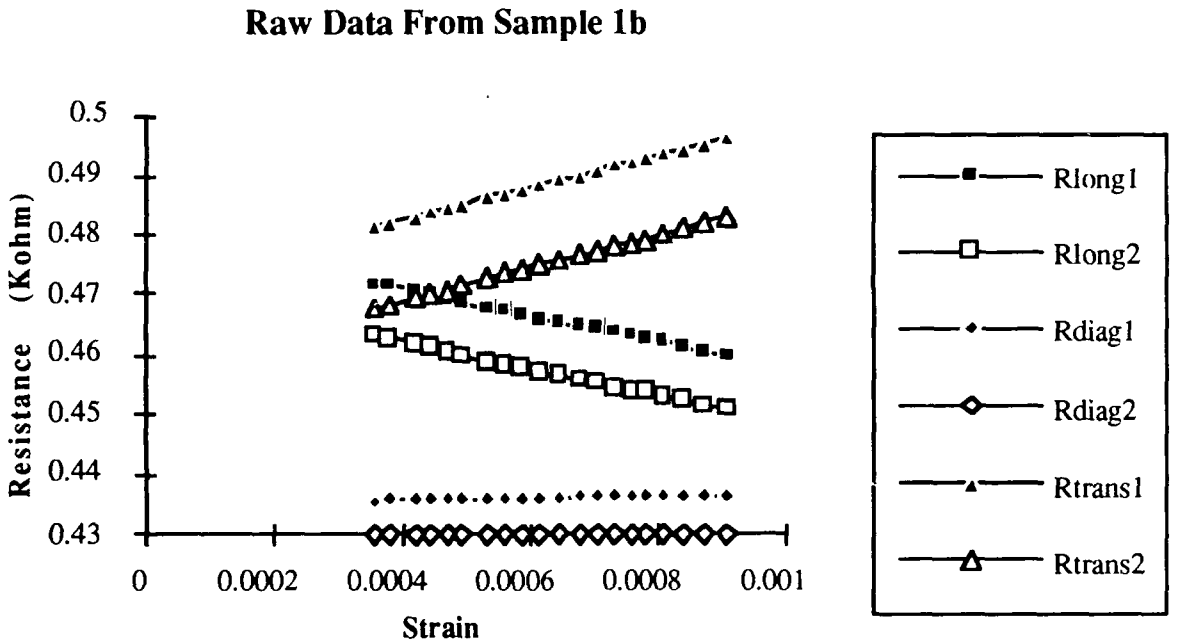


Figure 5. Raw data from sample 1b showing the resistance as a function of strain for the longitudinal, diagonal and transverse resistors.

In this study, the temperature coefficients of the resistance(TCR) and gage factor(TCG) were also examined. Our results are referenced to the their respective values at room temperature so

$$TCR = \Delta R/R(25°C)/°C, \text{ and}$$
$$TCG = \Delta G/G(25°C)/°C.$$

Since the room temperature data were not necessarily collected at exactly 25°C and interpolated value based on a linear fit was used.

3.1.4) Results

In figure 6 we show a plot of the gage factor versus the dopant density. Data for bulk silicon is also shown. From the figure, it is apparent that the ISE[tm] material has the same gage factor as bulk silicon. In results reported on laser recrystallized silicon[1], the longitudinal gage factor was significantly greater than the transverse gage factor. Our data show essentially equivalent values and more importantly show a very low value for the diagonal resistor. This can be important in many applications where the diagonal resistor may be used as a temperature monitoring device. In poly silicon[2] the gage factor has been determined to be about 1/3 that of bulk for the longitudinal resistor which is again nearly three times as sensitive as the transverse resistor. In a typical device applications, the transverse and longitudinal resistors are used in a resistive bridge configuration, taking advantage of the equal but opposite sign of the gage factor for each type.

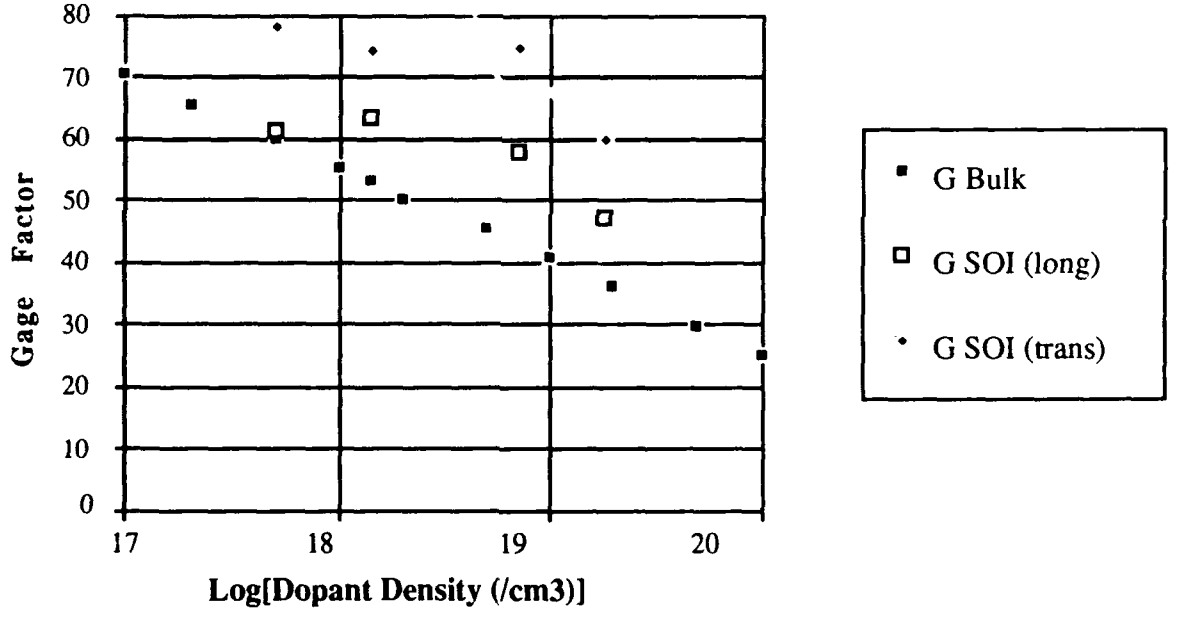


Figure 6. Gage factor vs. Dopant Density for ISE[tm] silicon in comparison to bulk.

In figure 7 a plot of the temperature data collected on one sample is shown. The relatively large amount of variation is due to the fact that the experiment was conducted in a simple oven with proportioning temperature control and to the difficulty that arises when trying to measure the sample temperature indirectly. Given these constraints the data are quite good. A plot of the TCR versus dopant density is shown in figure 8. Results for bulk are also plotted.

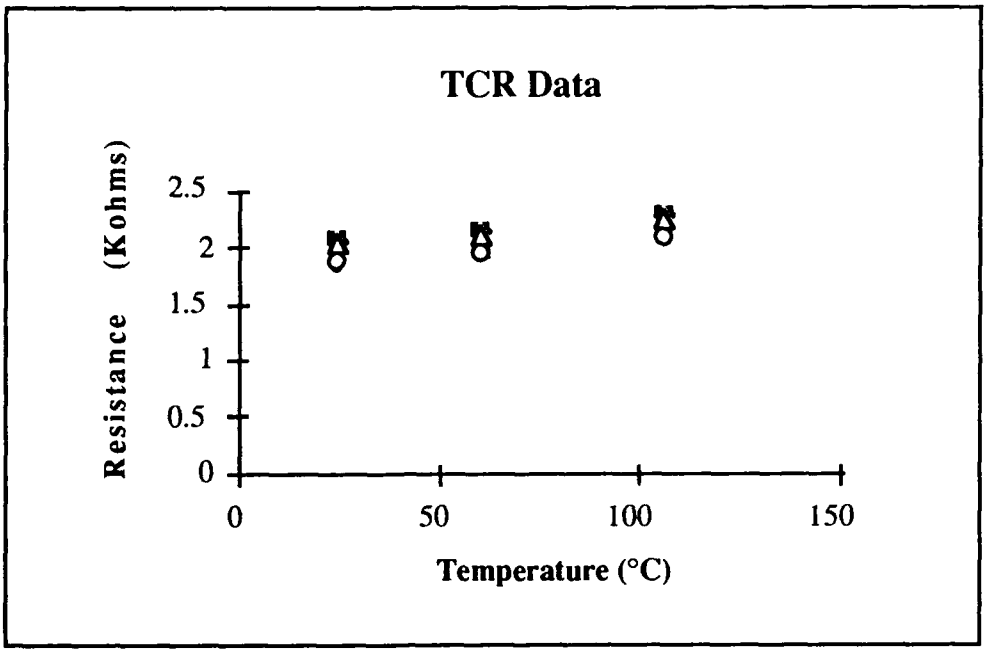


Figure 7. A plot of the temperature dependence of resistance for sample 3b.

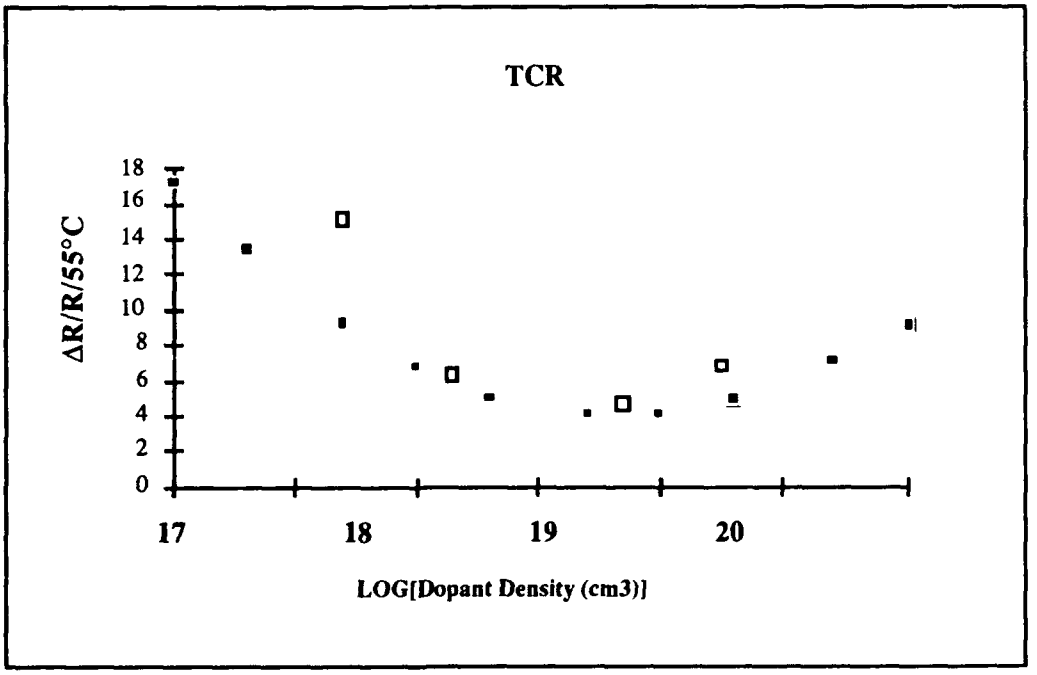


Figure 8. The dependence of TCR on dopant density.

The final graph (figure 9) shows the dependence of the gage factor on temperature as a function of the dopant density. Again the results are compared to bulk.

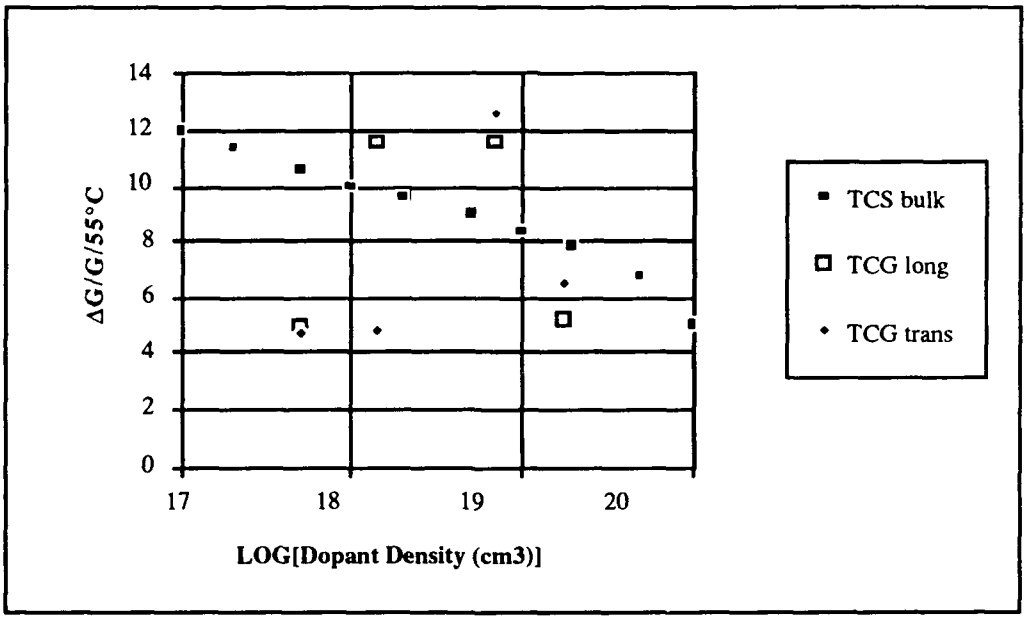


Figure 9. Dependence of the Temperature Coefficient of the Gage Factor (TCG) on Dopant Density.

3.2) Stress measurements

Wafers were prepared using a strain diagnostic mask set in order to evaluated the strain in SOI films. The majority of the strain diagnostic structures are similar to the ones reported by Henry Guckel and David Burns of the University of Wisconsin[3]. In addition, we have included the spiral structures reported by Richard Muller at the University of California, Berkeley[4]. Five three inch wafers were evaluated from two separate lots. Each wafer contained four sets of diagnostic structures placed in the four quadrants of the wafer. Each set of structures contain identical subsets oriented at 90° relative to one another and either perpendicular or parallel to the flat. The following table summarizes our results.

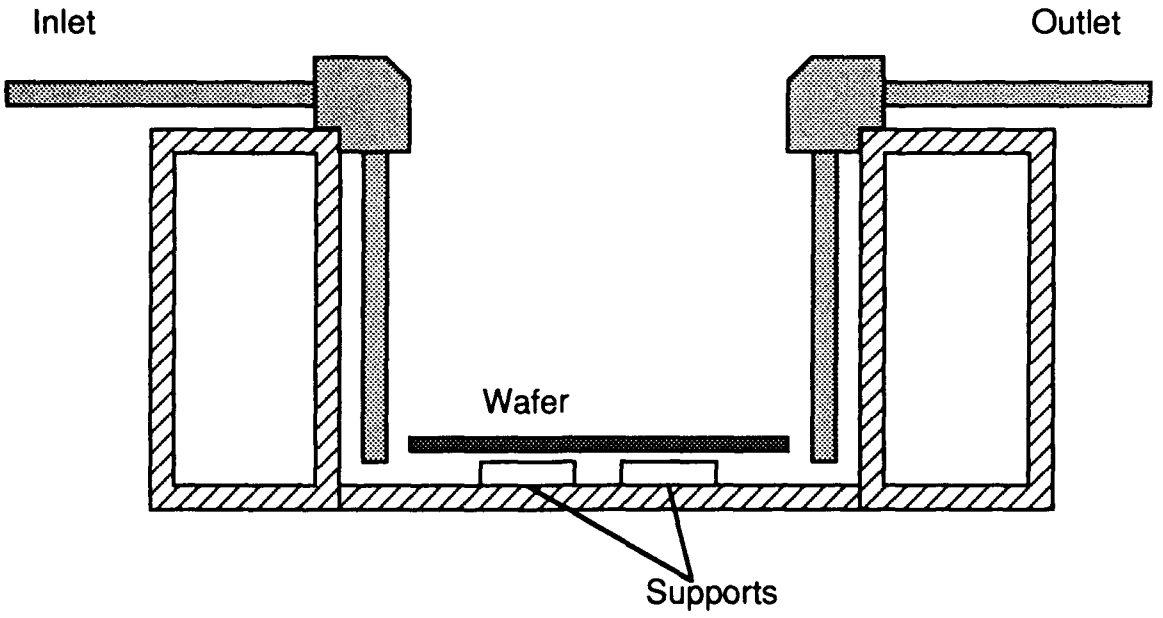
Table 1

No orientation dependence was observed
No correlation to position was observed
The measured stress was
1.8×10^8 dynes/cm^2
tensile
The Stress is uniform across the film thickness

3.2.1) Sample Preparation

Wafers were processed by first spinning on Shipley S1813 photoresist at 6000 rpm for 60 seconds. Samples were pre-baked at 95°C for 15 minutes. They were then patterned in a contact aligner. Resist developing was performed in batch fashion in a Teflon boat using Shipley Microposit MF319 developer at room temperature for 1.0 minute. Wafers were then rinsed and dried. Hard baking conditions were 105°C for 15 minutes.

We used a custom build RIE etcher with an SF_6/O_2 mixture to define the epitaxial silicon structures on the wafer. The buried oxide was used as an etch stop in the process. After etching, the resist was stripped in PRS 1000 at 95°C for 10 minutes, then rinsed and dried. The buried oxide was then undercut etched to release the mechanical test structures used for stress analysis. This process was conducted in a specially designed etching tank which is provided with a pump to introduce various etchants and an aspirator to remove the liquid from within the container. Only a single wafer can be processed at one time. The wafer is supported on mechanical rests which raise the wafer above the bottom of the container as shown below.

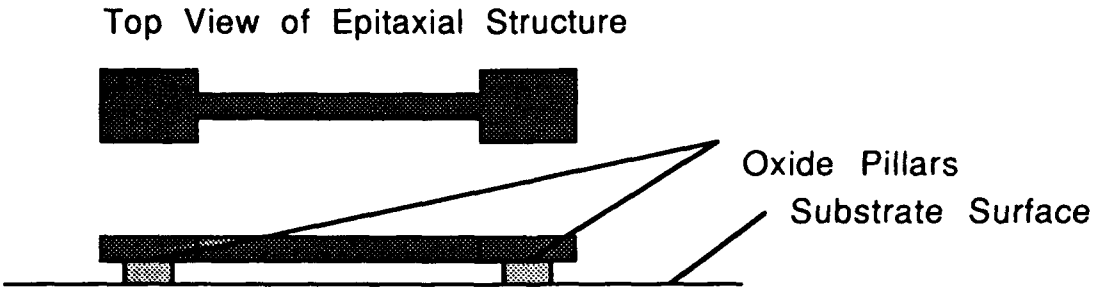


The wafer is inserted such that the surface faces down toward the bottom of the container. For this process, 49% HF is introduced into the container and the sample is etch for 20 minutes. This is sufficient time to undercut the epitaxial silicon structures (10 micron undercut is required). The HF is aspirated to a level just at the lower surface of the wafer such that the wafer is not allowed to dry. DI water is then pumped into the container at a low rate (200cc/min) while at the same time, the aspirator is turned on. This rinse procedure continues for fifteen minutes.

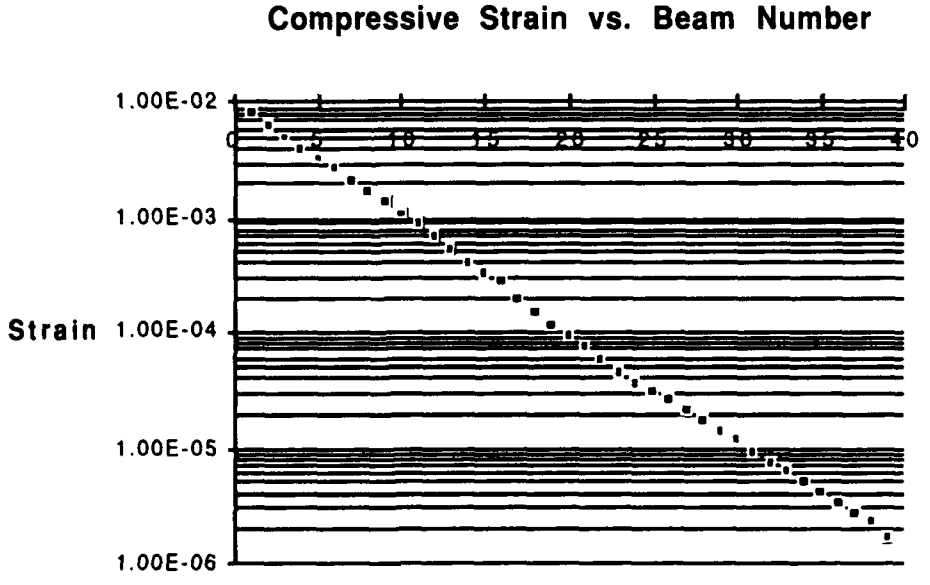
Since we intend to observe the samples wet, the next step is to turn the wafer surface hydrophilic. This is accomplished by introducing hydrogen peroxide at full strength into the container. The container which originally held about 200cc of DI water is now filled to 400cc to create a 50% peroxide solution. This is left for 1 minute and then diluted with DI water in the same manner described previously. The samples are now carefully removed from the container and placed in a petri dish which is partially filled with DI wafer.

3.2.2) Analysis

The mask set contains a variety of structures of differing sizes. To analyze compressive stress we used a doubly supported beam as shown below.



Buckling theory as outlined by Burns[5] in his thesis predicts a minimum strain required before the beam will buckle. By creating a mask set with a large number of beams, one can view the array of beams optically and observe buckled beams and use the length of the shortest buckle beam as an indication of the strain. The microscopic observation is aided by optical interference which occurs between the beam and substrate making buckled beams clearly visible. The plot below shows the range of stresses measurable with our mask set which contains 34 doubly supported beams which range from 20 to 1400 microns.



If the films are under compressive stress, then the beams will buckle at lengths greater than some critical length. The critical strain for buckling is given by:

$$\varepsilon_0 = -\pi^2/3(h/L)^2,$$

where

h = the thickness of the beam, and

L = the shortest length beam to buckle.

Assuming bulk silicon properties, the stress can be evaluated from

$$\sigma_o = E\varepsilon_o/(1 - \nu),$$

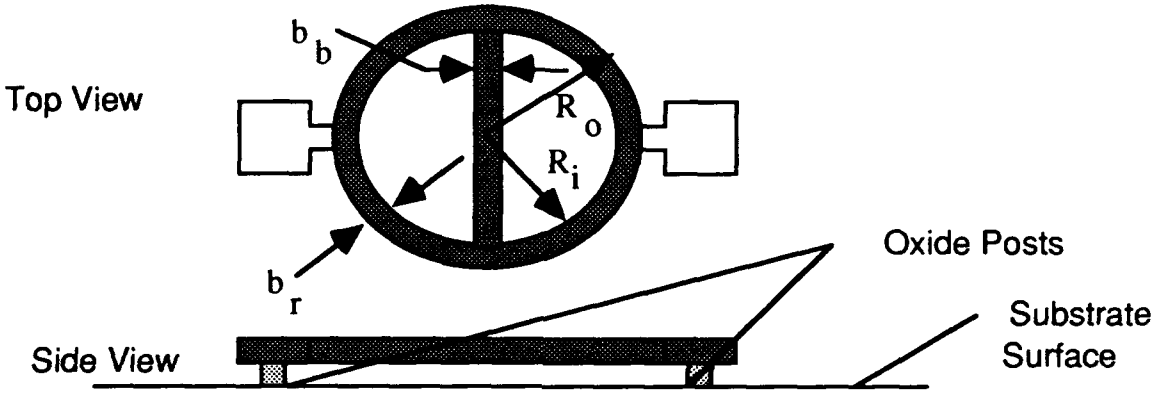
where

E = Young's modulus (1.6×10^{12} dynes/cm^2),

and

ν = Poisson's Ratio (.28).

The second buckling structure is used to evaluate tensile stresses is shown below.



Let b_b be the width of the connecting beam, and R_i and R_o be the inside and outside diameters of the ring. Finally, let b_r be the width of the ring which is equal to R_o - R_i, of course. Under conditions of tensile stress, the thick outer ring dominates the mechanical behavior of the structure. Since the film is under tensile stress, it will shrink when released from the substrate. Because the ring is clamped at two points it can only shrink in the direction of the connecting beam, causing the center connecting beam to buckle. The determination of tensile strain from observations of rings of different geometries is slightly more complicated than for the simple bridge structures. In fact, because the support conditions for the center beam are neither clamped or supported, only limits for the minimum and maximum strain are available. They are

$$\frac{\pi^2 h^2}{12\, g(R)\, (2R_{cr})^2} \geq e_o \geq \frac{\pi^2 h^2}{2\, g(R)\, (2R_{cr})^2},$$

where

R_{cr} = the critical radius at which buckled beams are first observed,

g(R) = is a geometric factor that can be derived from the equation,

$$g(R) = \frac{-2\, b_r f_2}{2b_r f_1 + b_b f^2 - b_b f_2^2},$$

where

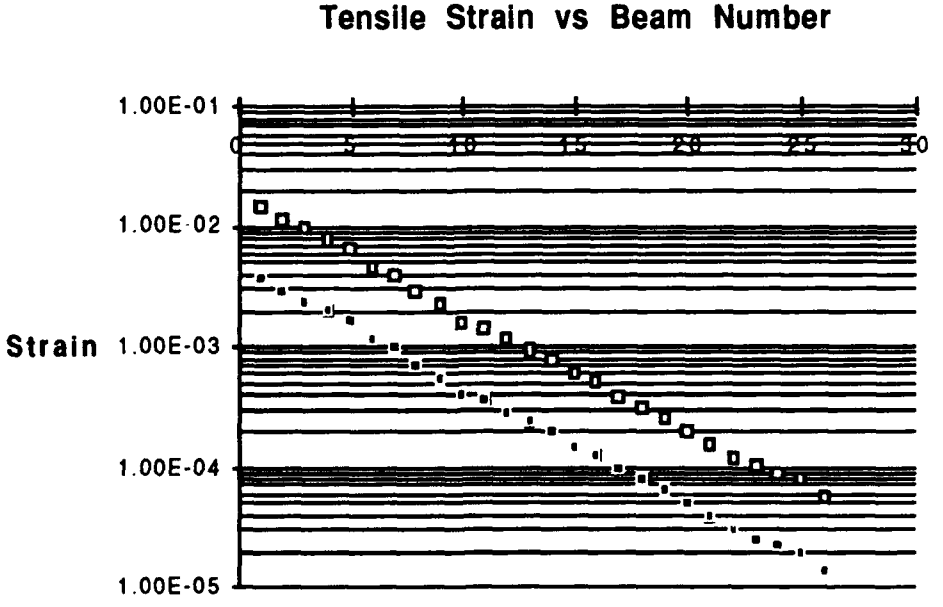
$$f_1 = (\pi/4 - 2/\pi)R/e - 2e/\pi R + 4/\pi - \pi/4 + \pi k(1 - \nu)/2$$

$$f_2 = (1/2 - 2/\pi)R/e - 2e/\pi R - 1/2 + 4/\pi - k(1 - \nu),$$

where k is the form factor (k = 1.2 for rectangular cross- sections) and e is the eccentricity

$$e = R - b_r/\ln(R_o/R_i).$$

Using this analysis the range of tensile strains measurable with our mask is shown below.



3.2.3) Spiral Structures

Spiral structures are useful in the determination of the variation of strain with film thickness. These devices were reported by Muller, et al[6]. The technique involves the same processing as

described above where in the shape of the epitaxial structure created is a spiral either anchored at its center or at an edge. A variation of the stress as a function of the thickness of the material causes the spiral structure to curl up or down depending on the sign of the stress gradient. Thus when curling upwards, the center mounted spirals can be used to analyze the stress. Graphs presented in their paper provide the relationship between the rotational angle, the lateral contraction, the height and the strain gradient.

3.2.4) Results of Strain Measurement

An analysis of the strain in ISE^{tm} SOI films was conducted and revealed that the strain in ISE^{tm} is uniform to the detection limit of our measurements and that tensile stress was observed at a level of about $2x10^8$dynes/cm^2. It was further found that the stress is uniform with respect to position and orientation on the wafer. Only two orientations were tested; normal and perpendicular to the (110) direction.

IV) PROCESS DEVELOPMENT

4.1) Overall Process

Our basic concept is depicted in figure 10. The process begins with a standard ISE^{tm} SOI wafer. Starting with a standard SOI wafer has advantages. It frees the sensor manufacturer from having to run the ISE^{tm} process at his facility, and therefore increases the number companies that could use the process developed under this contract. It also avoids the problem of wafer distortion that occurs during the recrystallization process. This distortion limits the minimum feature size possible, due to alignment problems.

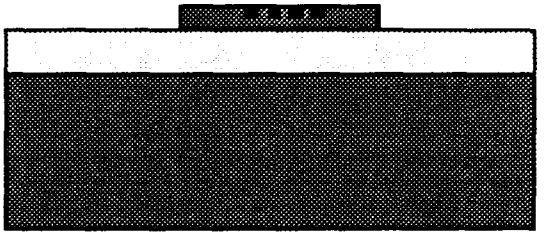
The ISE^{tm} epitaxial silicon layer is first patterned to define the diaphragm area. After etching the thin epitaxial silicon epitaxial film, the underlying oxide is exposed in those areas were the silicon epi has been removed. The oxide can then be etched. This process is performed wet, undercutting the diaphragms to some extent. Polysilicon is deposited next with the expectation that it will totally surround the edge of the diaphragm as shown in the figure. The oxide must be removed from beneath the diaphragm to free it. This aspect of our process will be discussed in greater detail in the next few paragraphs.

The most important and critical aspect of this new process, is that the polysilicon layer actually surround and adhere to the epitaxial silicon diaphragm. Before committing to this approach, Kopin prepared some samples using the mask set from Phase I. In figure 11a, a photograph of a test sample is shown. This photo was obtained by cleaving a sample such that the cleavage intersected the diaphragm. A slight oxide etch was performed to enhance the contrast between the poly, oxide and epitaxial layers, and the sample was prepared for the SEM. Figure 11b shows our interpretation of the SEM photograph. The oxide layer has been clearly delineated. It is about 3 microns thick. While it is difficult to see, the single crystal silicon diaphragm layer protrudes out over the edge of the oxide region indicating the extent of the undercut during the oxide etch. The polysilicon, which looks somewhat lighter than the epitaxial silicon in the picture has surrounded the protruding epitaxial layer and is conformal with the oxide layer. This result indicates that the use of polysilicon as a clamp is well justified.

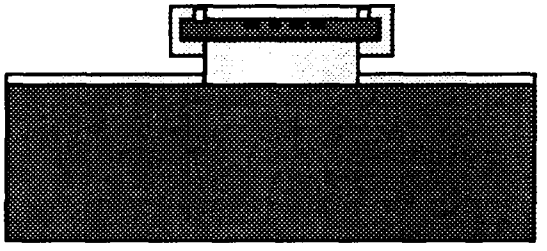
1) Implant p- and p+ regions and activate

2) Pattern and etch siicon epi layer.

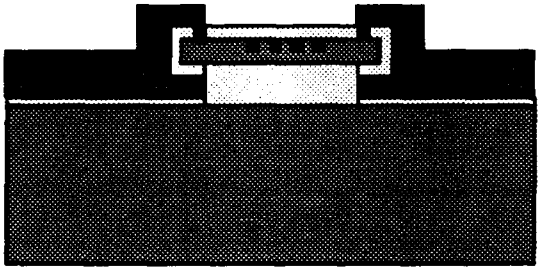
3) Etch underlying oxide layer.



4) Reoxidize the wafer and pattern oxide fro poly anchors.



5) Deposit and pattern polysilicon. The polysilicon will be used to support the silicon diaphragm.



6) Etch thin oxide and underlying oxide in concentrated HF.

7) Reseal diaphragm by oxidizing the silcon diaphragm and poly silicon support.

8) Thin metal and shield.

9) Thick metal deposition and pattern.

10) Oxide etch.

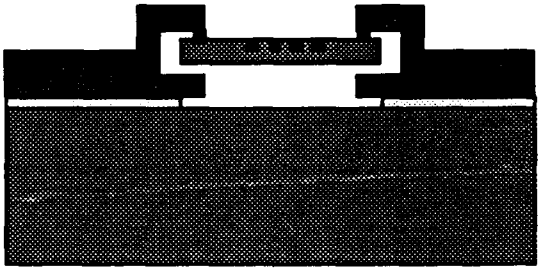
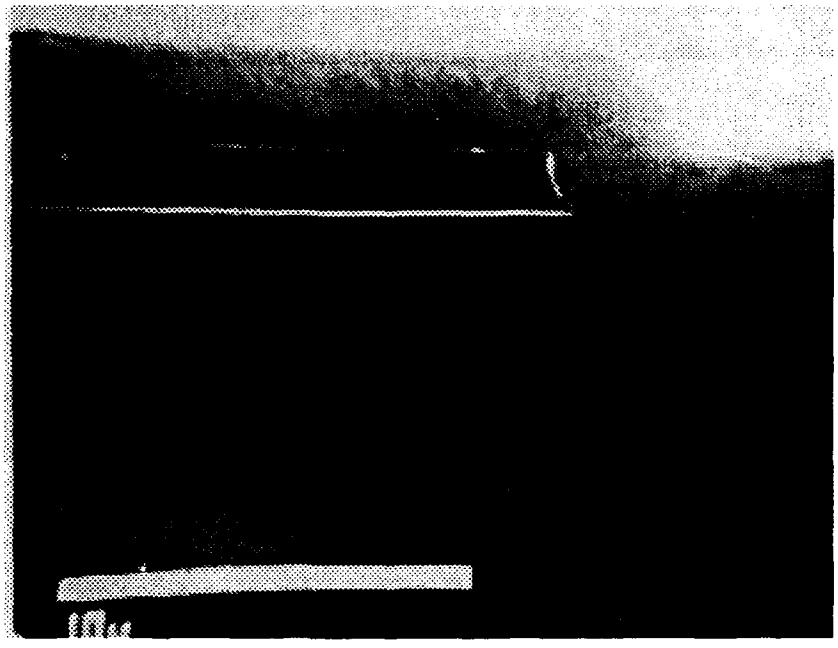


Figure 10. The simplified pressure sensor process flow.

a)



b)

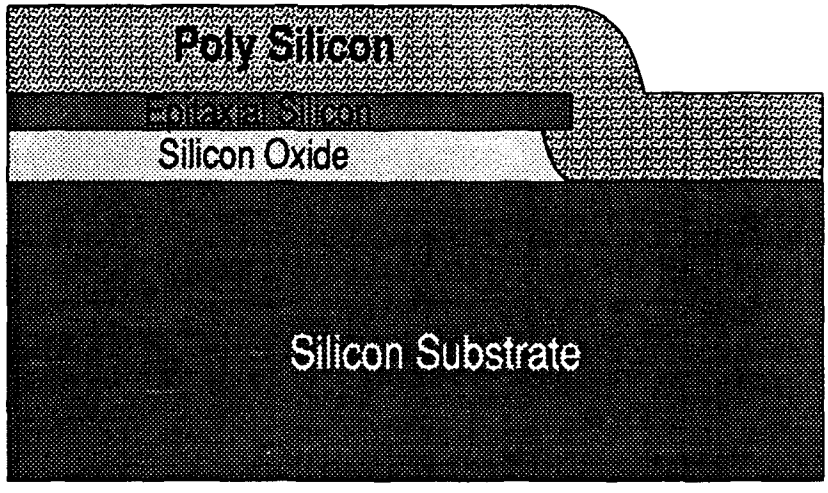


Figure 11. a) SEM photograph of the polysilicon step coverage at the edge of the diaphragm. b) Drawing showing our interpretation of the SEM image.

To understand in more detail the process for etching the oxide out from beneath the diaphragm we have created the illustration shown in figure 12. After the epitaxial diaphragm has been defined, it will be reoxidized slightly. This oxide will be etched to create anchor points in the top of the diaphragm. These are places were the subsequent polysilicon deposition will come directly in

contact with the epitaxial silicon. We call them anchors because they will be used to support the diaphragm during subsequent processing. After the poly has been deposited, it can be patterned, and the oxide on the epitaxial diaphragm can be used as a stop to prevent the diaphragm from being etched during the poly etch process. With the poly supports defined, the wafer will be immersed in a concentrated HF bath. The HF will etch the thin oxide between the poly support and the epitaxial silicon. The etching will continue around the edge of the protruding portion of the diaphragm and finally into the underlying oxide. With enough time in the bath (2hr), the HF will completely remove the oxide from beneath the diaphragm. At this point, the diaphragm is supported at the anchor points. To reseal the diaphragm, the wafer is oxidized. Oxide forms on all silicon surfaces (poly support and the epitaxial layer), eventually merging together and sealing the cavity. If the oxidizing ambient were pure oxygen, then the oxidation process would continue under the sealed diaphragm until all the oxygen was consumed and converted to silicon dioxide This would create a vacuum inside the sealed cavity. The sensor made using this process would be an absolute pressure sensor. Different ambients could be used during oxidation. For instance, argon could be added. The final pressure inside the sealed cavity would depend on the percentage of argon in the oxidizing ambient.

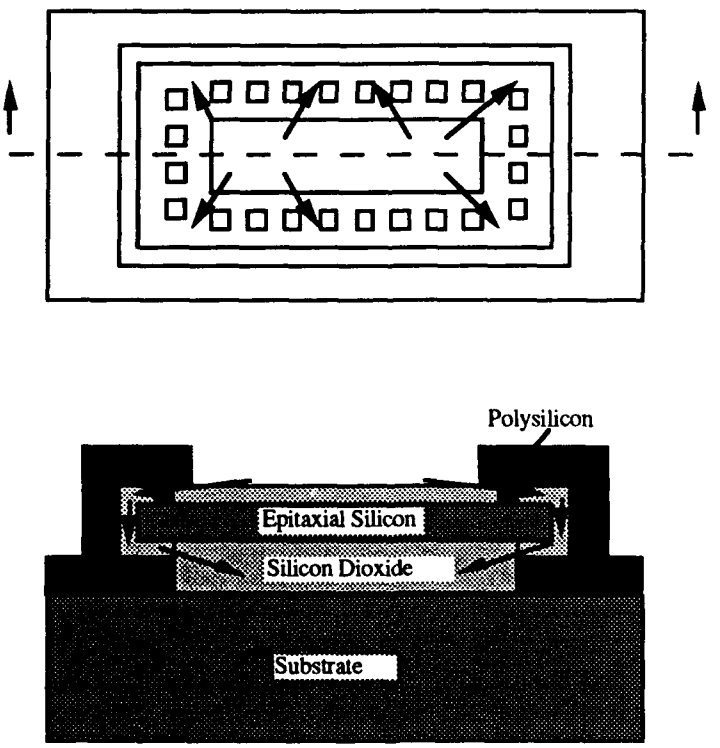


Figure 12. Detail of the oxide undercut process. The arrows show the path of the HF etchant.

4.2) Diaphragm Release Methods

One of the most critical aspects of this process is the method used to release the diaphragms. As described above the cavity is formed by etching the oxide beneath the diaphragm. Problems arise when one attempts to remove the liquid from beneath the diaphragm. It was found that in removing a wafer from an HF bath, the HF solution would drip out from beneath the diaphragms. For a small diaphragm, one 100μm or less on a side, this procedure was adequate to produce freely suspended diaphragm structures. However, it was observed that for larger structures, >100μm, the process left the diaphragms stuck to the substrate. Microscopic observation confirmed our suspicion that capillary action was drawing the diaphragm down to the substrate as the liquid was evacuating the cavity.

Kopin embarked on a program to develop a procedure that would insure that even the largest diaphragm structures would be free. The following paragraphs report three of the methods explored by us.

4.2.1) HF Vapor Etching

This process was originally attempted during Phase I of this program. The results were unimpressive. The approach taken at that time was to heat a bath of HF to near the boiling point. A wafer was supported on a holder made of an organic material resistant to the HF etchant. The wafer was inverted, so that it faced downward and placed on top to the hot HF bath for a predetermined period. The wafers were then removed from the etching apparatus. Microscopic examination of the diaphragms indicated that they were indeed undercut and at a rate essentially equivalent to that observed with immersed samples. However, liquid condensed on the sample surface and therefore undermined the intent of the process.

During Phase II, we revisited this process. Our Phase II results are much more impressive. We re-examined the etching configuration and developed a set-up shown in the photograph in figure 13. This set-up consists of a hot plate, a vacuum chamber and shower head. For safety reasons, we continue to extract HF vapors from a hot HF bath (49% HF in water). The sample is placed on the hot plate and heated to about 200°C. A polypropylene tube connects the shower head to a covered HF bath container. This container has a port for extracting the vapors and an input port which regulates the flow of air into the system. The HF vapors enter the vacuum chamber through a tube at the top and are drawn out the sides as shown in the diagram in figure 13. The exit ports of the vacuum chamber are connected to a venturi which creates a slight vacuum and draws the vapors through the chamber, combines them with water and releases them into our chemical drain.

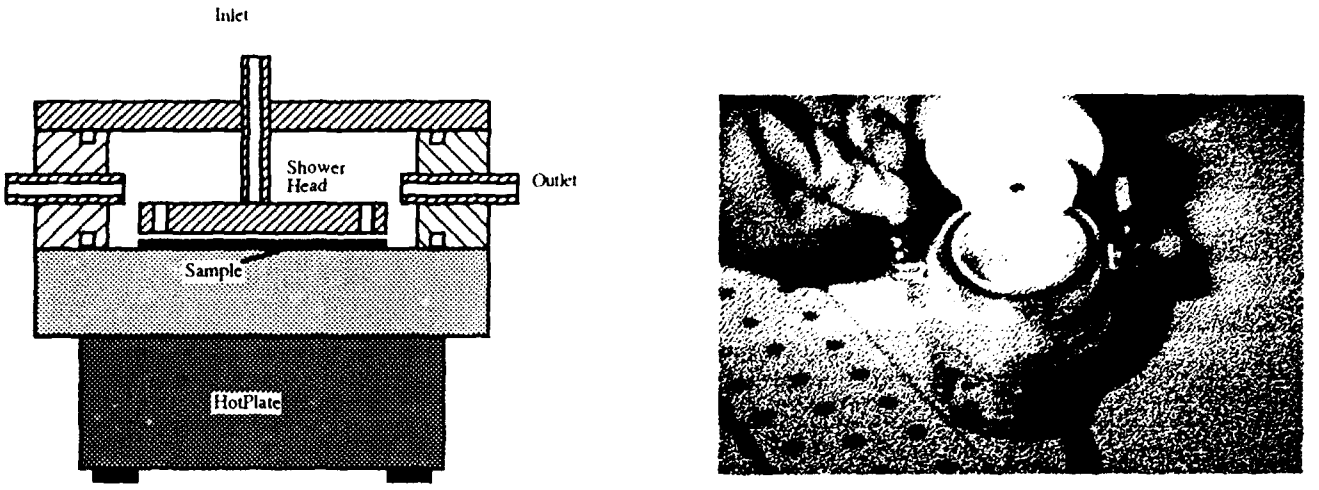


Figure 13. Vapor HF etching set-up.

The results obtained with this process have been very encouraging. Using a mechanical test mask shown in figure 14, we have achieved success freeing very long(several hundred microns) cantilever beams. The photographs in figure 15 snow some of our results.

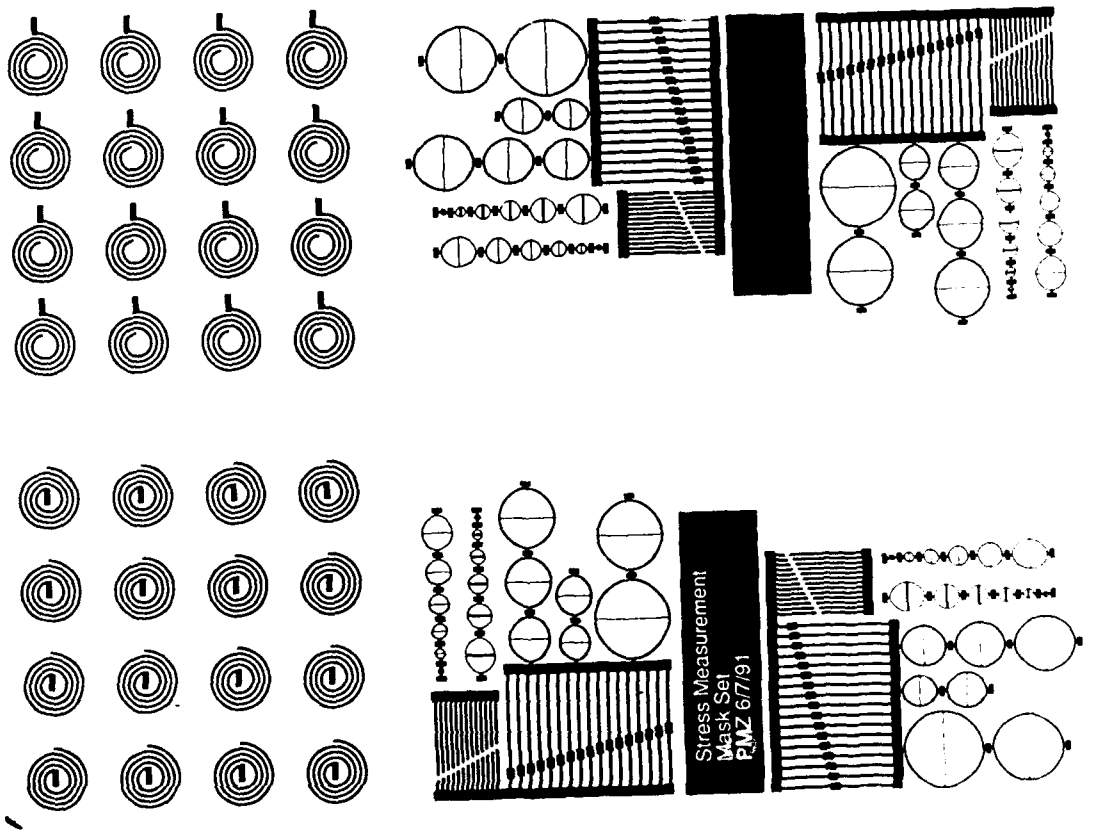


Figure 14. Mechanical Test Mask

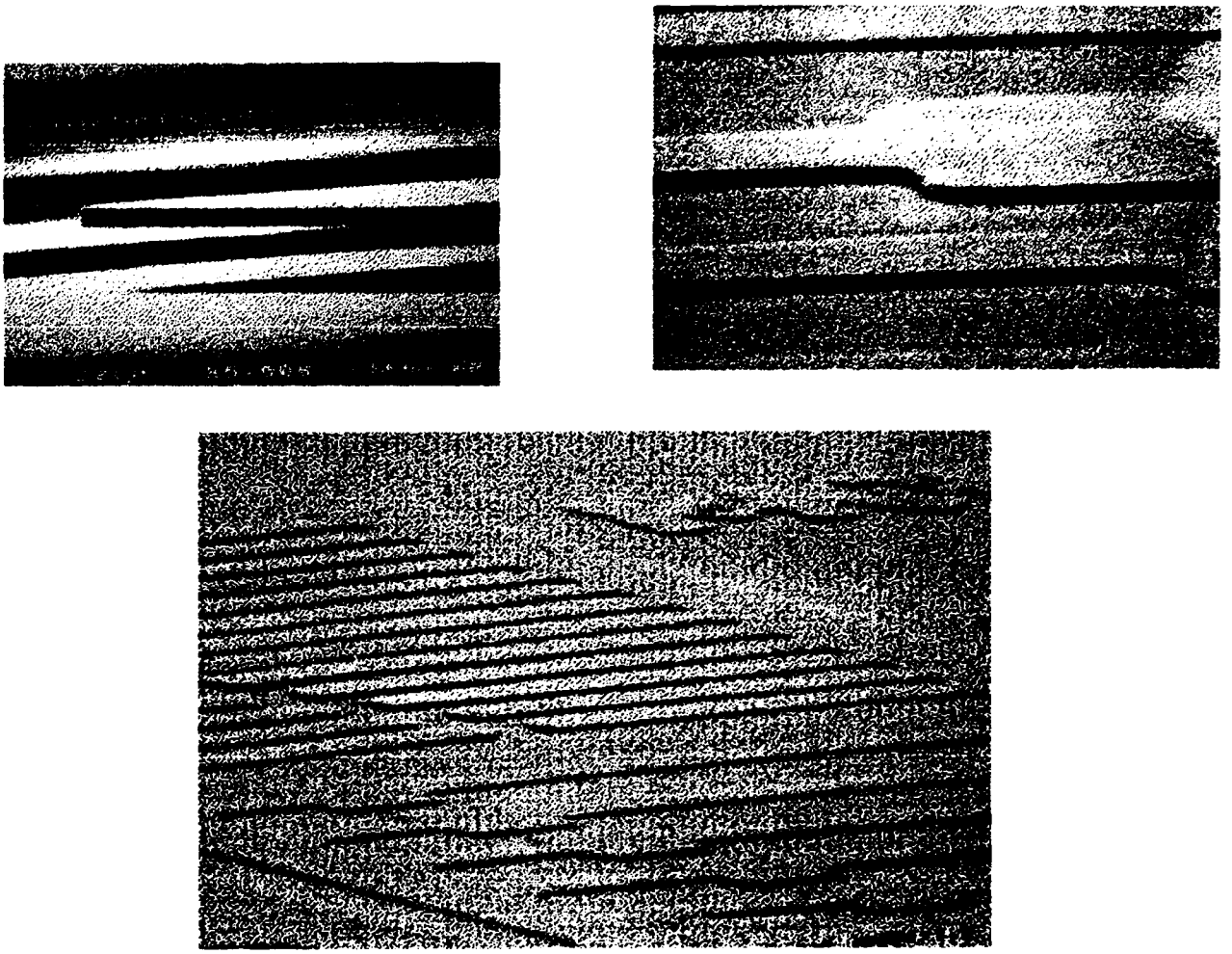


Figure 15. Photographs of undercut structures.

A remaining disadvantage of this process is that there appears to be a residue left on the wafers after processing. The origin of this residue is unknown at this time, but we suspect that it may be an organic material. It has been difficult to remove even in wet etches. A second disadvantage is that this process is significantly slower than straight HF etching.

4.2.2) Sublimation

During Phase I we also reported a technique we refer to as the sublimation process. In this process, the wafer is kept wet after rinsing and placed into a freezer. When the water has frozen, the wafer is removed from the freezer and placed in a vacuum system. The idea, suggested by

Professor Henry Guckel is to cause the water to sublimate in vacuum or to go from the solid phase directly to the gaseous phase. This would be the equivalent of dry etching with the advantage that the process is totally selective. This concept has great appeal and on the surface may present a more production oriented process.

While the process with water can work, several issues arise. The water must be maintained in the solid state while under vacuum. If it should liquefy, the results can be very damaging. As a liquid under vacuum, the water will boil destroying the micromechanical structures. To avoid this problem, the wafer must be kept at a low temperature during the vacuum drying process. A second issue is that the micromechanical structures can be damaged or forced into contact with the wafer surface during the rinse process. In addition, the wafers must go from the HF to the rinse without leaving a liquid. If they are pulled directly out of the HF, they will dry immediately and be ruined.

To avoid the problems just mentioned, we developed an apparatus specifically for this process. It is shown in the photograph in figure 16. As can be seen, the system consists of a PVC container with a hollow side wall. An input tube delivers etchant or diluent to the container and an aspirator is used to remove the liquid from the container. The hollow walls of the container are filled with a liquid with a high specific heat whose purpose will become clear in the following paragraphs.

In use, the unetched sample is placed in the container. HF is introduced and the sample is etched to completion. The input tube is connected to a DI water source and rinse water flows gently into the container. The aspirator keeps the level of liquid in the container constant and just above the surface of the sample. Any number of liquids can be introduced into the chamber and flushed in this manner. Once the rinse cycle is complete, the container is essentially emptied of liquid by the aspirator. The last solution used must be one that can be made to sublimate under vacuum at reasonable temperatures and will not dewet the sample. Therefore, after the container is emptied, a puddle of liquid remains on the sample surface. The tubing is disconnected from the container and the container is placed in a freezer. This freezes both the liquid on the sample and the liquid in the walls of the container. Once frozen, the container is removed from the freezer, covered, and evacuated. The walls of the container remain cold for a long period of time while the frozen liquid on the surface of the sample sublimates.

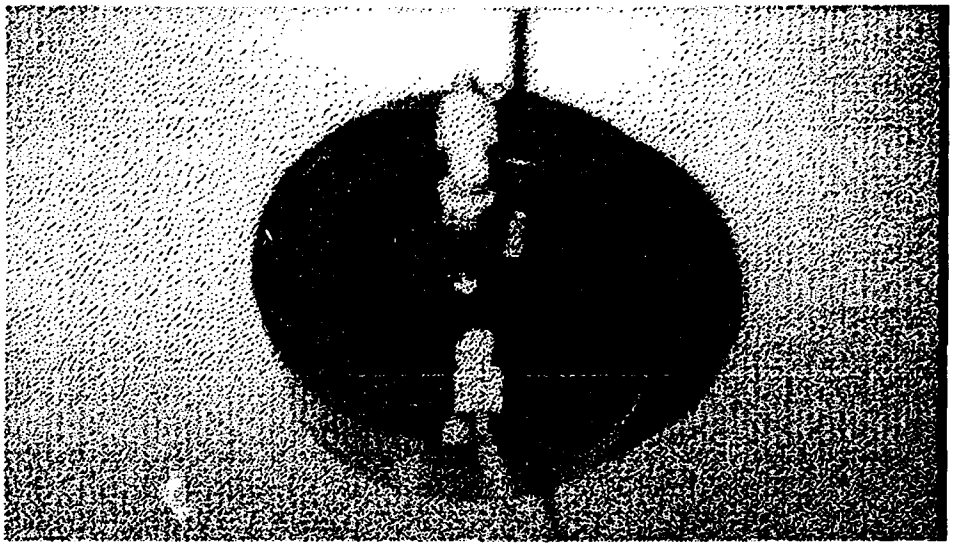


Figure 16. Photograph of apparatus used for sublimation.

The greatest difficulty with this process has been in keeping the sample frozen. Several liquids were tried with varying degrees of success. These include cyclohexane, water and acetic acid. Most of the effort has been expended on the cyclohexane process. Difficulties have arisen in trying to obtain pure cyclohexane on the surface of the sample at the end of the rinse process. The procedure was to go from HF to water to alcohol and finally to cyclohexane. Any alcohol remaining in the cyclohexane at the completion of the rinse cycle will segregate from the cyclohexane after freezing. If liquid is there during the vacuum process, the results are poor. A second problem with cyclohexane is that it too appears to leave a residue on the sample. Improvements in the grade of cyclohexane and filtering may decrease this problem.

4.2.3) Alcohol Displacement and Vaporization

Experiments with drying seemed to indicate that as the liquid is removed from beneath the mechanical structures, capillary action of the liquid draws the structures toward and finally into contact with the substrate. Alcohol was first tested with air drying, in an attempt to reduce the sticking problem by reducing the surface tension between the evaporating liquid and the mechanical structure. Better results were achieved with alcohol than with water, but the process was still not adequate for structures greater than 100 microns. We are certain that capillary action is the dominating effect in pulling the beams toward the substrate. It therefore seemed reasonable to seek a force which could compensate that due to surface tension. In this approach we counteract capillary action with gas pressure that is generated by rapidly evaporating the alcohol.

The process begins by displacing the HF solution with water and subsequently with alcohol. The alcohol is then rapidly evaporated off the surface using a hot plate. This simple procedure provided very reproducible results. All the structures on our mask set were free standing after this process including the spirals.

4.3) Results of Fabrication

The process as describe in section 4.1 for fabricating single crystalline silicon pressure sensors was used to make free standing silicon diaphragms. Free diaphragms up to 1000 microns on a side have been demonstrated.

After completing the initial fabrication steps through the patterning of the polysilicon clamping structures, the wafers were immersed in 49% HF to undercut the silicon dioxide and free the diaphragms. After thoroughly rinsing with water, the devices were examined to be sure that the silicon oxide had been completely etched. This examination took place under water and indeed the diaphragms were free of the substrate. The alcohol displacement and vaporization process was used to produce free diaphragms in air. Since the diaphragms are nearly completely enclosed, the amount of pressure required to prevent them from being drawn to the substrate during drying is significantly less than for the beams describe previously and lower hot plate temperatures are employed. It also appears that some concern must be given to the range of diaphragm sizes on a given die. We found that since the larger devices are more pressure sensitive, that lower vaporization temperatures are required. On our die, we have four different size diaphragms ranging from about 100μm square to 1000μm square. The pressure sensitivity for the smallest is 1000psi while the largest is 0.1psi. We were able to free all structures simultaneously. Further increases in the range may not be possible, especially at the low pressure range.

Figure 17 shows a top view of a complete 1000x700μm^2 diaphragm. Structures such as this one were examined under a probing station. The probe which is normally used to make a contact with an electrical bond pad had a blunt tip that was support by a mechanical holder capable of providing xyz motion. The tip was brought into contact with the surface of the diaphragm. Continued pressure pushed the diaphragm into the substrate and when the probe pressure was released the diaphragms rose with it. This demonstrated that the diaphragms were indeed free. It had also been a concern that once the silicon diaphragm contacted the surface it would stick. We did not observe this problem.

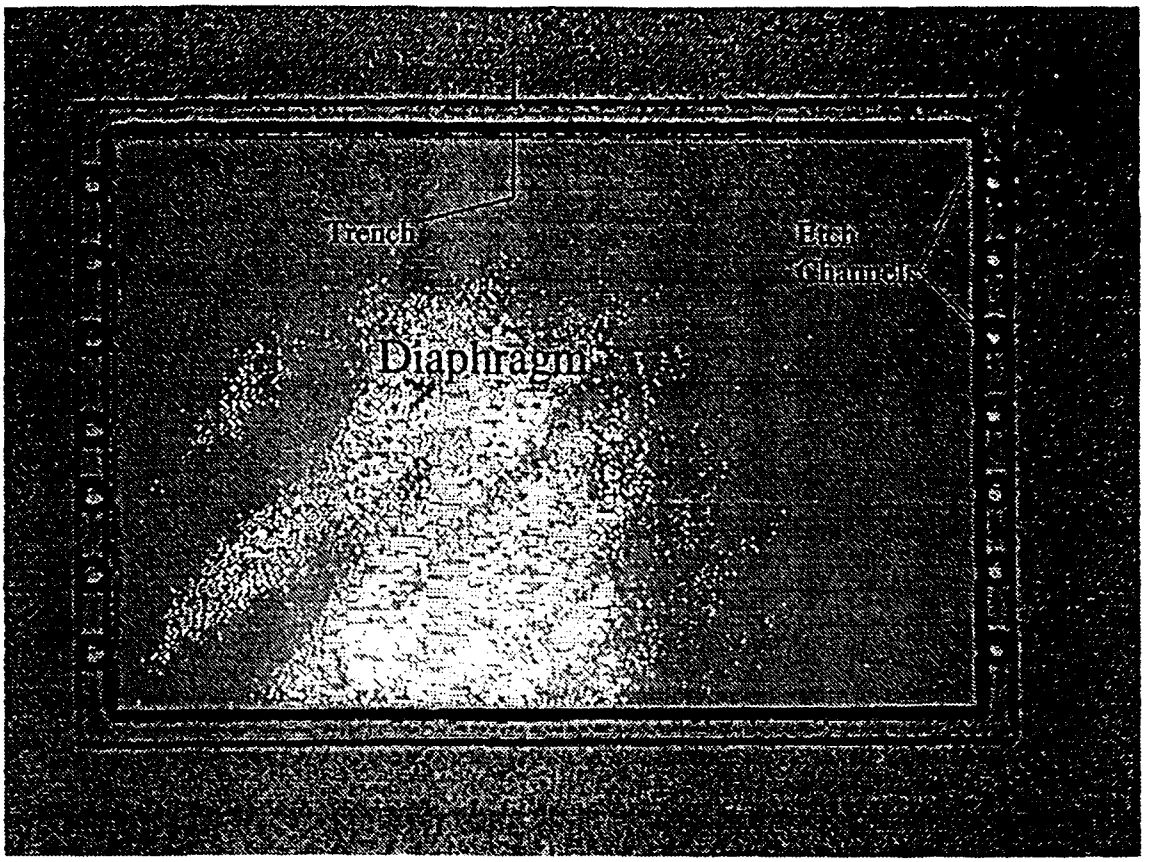


Figure 17. Photograph of a fabricated single crystalline silicon diaphragm.

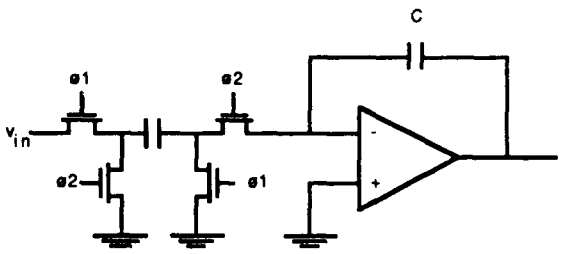
Our future plans require us to seal the cavities using the methods outlined in our proposal and metallize the devices for measurement.

V) CIRCUIT DESIGN

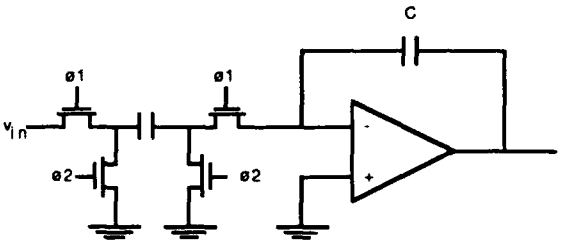
5.1) Overview of the Transducer Circuit

A transducer circuit investigated during this program is based on the inverting and non inverting switched capacitor integrators below. These circuits are very standard building blocks in the design of switched capacitor filters. They can be understood and analyzed simply as charge control amplifiers. Through the use of a two phased clock the circuits charge a test capacitor and transfer the charge onto the integrating capacitor. When these circuits are combined as in the transducer circuit below, they make a simple yet elegant capacitance measurement circuit.

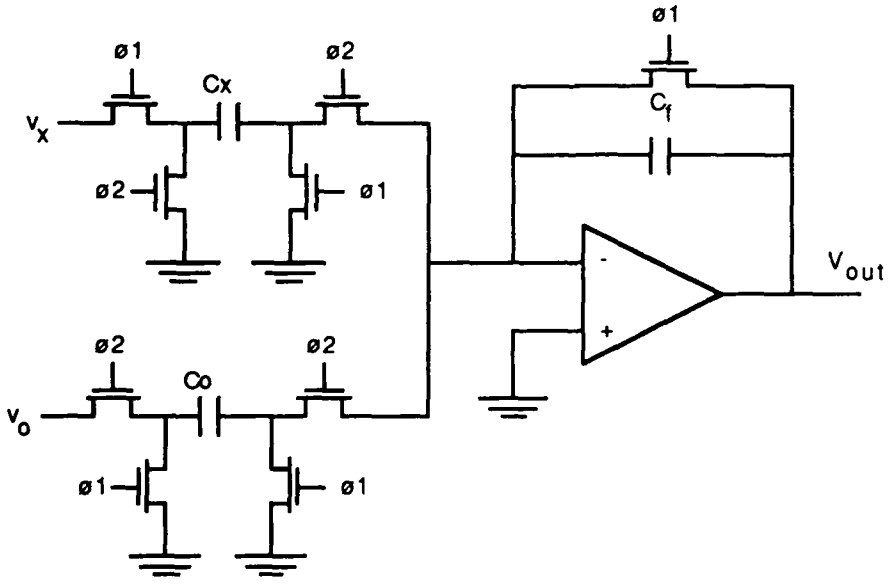
NON INVERTING



INVERTING



THE TRANSDUCER CIRCUIT



A change is made in the inverting integrator clock phase to allow the measure and reset cycle to be completed in only two phases rather than the three phases that would otherwise be needed.

Phase I: Capacitor C_x charges to V_x while C_o and C_f are discharged.

Phase 2: C_x discharges to 0 volts. As a result, a charge C_xV_x is drawn from capacitor C_f.

Capacitor Co charges to V_o resulting in a charge C_oV_o flowing into C_f.

$$V_{out} = (C_xV_x - C_oV_o)/C_f$$

The resulting output voltage is proportional to measure capacitor C_x. The zero and span are independently adjustable by control voltages V_o and V_x. For example, if C_x has a range from 10 to 20pF, C_f and C_o are chosen to be 10pF and $V_x = V_o = 10V$ then V_{out} will have a range from 0 to 10V. One modification that was considered was to replace the integrating capacitor with a current mirror. The current mirror has a temperature independent current gain equal to the ratio of (W/L) of the output device to (W/L) of the input transistor. The op amp is retained to provide a low impedance node for discharging the capacitors. The gate-source voltage of the MOSFETs will be divided by the open loop gain of the op amp so that the capacitors will "see" nearly zero volts at the op amp input. Elements of the op amp used in both of the circuits describe above are considered below.

5.2) Circuit Analysis

In order to understand the operation of the transducer circuit, we will provide some background into the operation of circuit elements required.

5.2.1) MOSFET

A MOSFET's I-V characteristics can be described in two regions of operation as:

TRIODE ($V_{ds} < V_{gs} - V_t$): $I_d = K(2(V_{gs} - V_t)V_{ds} - V_{ds}^2)$,
$K = 1/2C_{ox}\mu_n(W/L)$.

PINCH OFF ($V_{ds} > V_{gs} - V_t$): $I_d = K(V_{gs} - V_t)^2(1 + V_{ds}/V_a)$,
$r_o = V_a/I_d$, and V_a is the Early voltage.

The transconductance is simply the change in the current flowing from the source to the drain as a function of the gate bias when the transistor is operating in the pinch-off or saturation region.

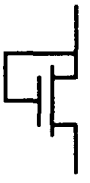
$g_m = 2K(V_{gs} - V_t)$, $g_m = 2I_d(V_{gs} - V_t)$, $g_m = (2.\mu_n C_{ox} W/L I_d)^{1/2}$,
$g_m = \partial i_d/\partial v_{ds}|_{vgs=const.}$

Transconductance is proportional to the aspect ratio and to the amount the bias voltage exceeds the threshold voltage (V_{gs} - V_t). Transconductance for a given device is proportional to the square root of the bias current. At a given bias current transconductance is proportional to the square root of (W/L). For typical values of I_d = 1mA, C_{ox} = 20μA/V and (W/L) = 100: g_m = 2mA/V.

A BJT operating at 1mA will have a $g_m = I_c/V_t$ = 40mA/V. Redeeming features of MOSFETs are high input impedance, low power dissipation, small size and ease of fabrication.

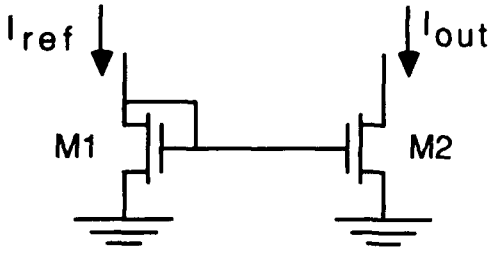
5.2.2) Diode Connected MOSFET

Since $V_{ds} = V_{gs}$ for this circuit the device is either cut off (for $V_{gs} < V_t$) or is in the pinch off mode (for $V_{gs} > V_t$).



5.2.3) Current Mirror

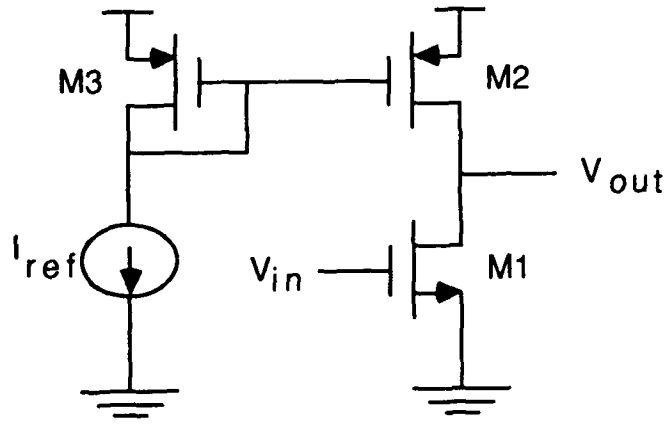
Current mirrors are used both to generate currents which are proportional to a reference current (for biasing) and as active loads so that high resistance loads can be implemented in small area. Two transistors that are fabricated together will have identical characteristics (V_T, K_p, etc.). A reference current can be established in a diode connected transistor as shown below. This sets up the gate voltage for a second transistor. If the transistors were identical in every sense, including their geometry, then the current I_{out} would be identical to I_{ref}, and thus the name "Current Mirror".



$I_{out} = I_{ref} (W/L)_2/(W/L)_1$

5.2.4) Single Stage high gain CMOS amplifier

Transistors M_3 and M_2 are a matched pair. M_2 operates in pinch off and acts as an active load. $r_{o1} = r_{o2} = V_a/I_{ref}$



$$A_v = V_{out}/V_{in} = -g_m(r_{01} \parallel r_{02})$$

with

$$r_{01}\|r_{02} = V_a/2I_{ref}$$

and

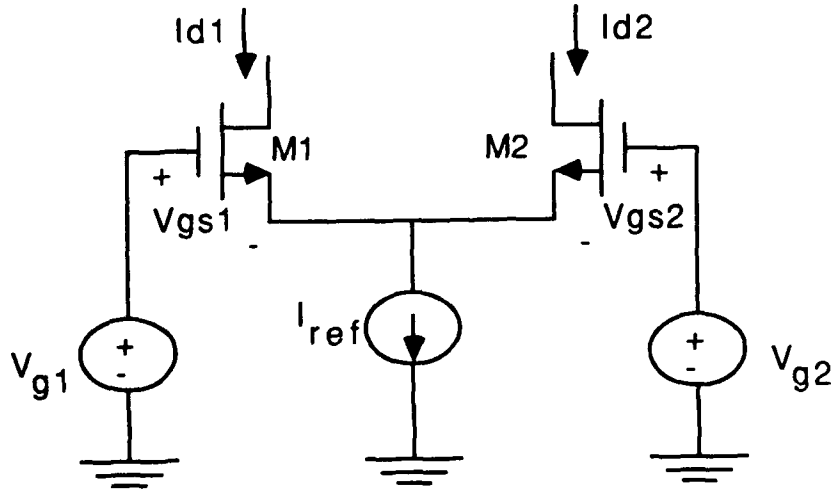
$$g_{m1} = 2(K_1 I_{ref})^{1/2}$$

then

$$A_v = -(K_1/I_{ref})^{1/2}|V_a|$$

Voltage gain is inversely proportional to the square root of bias current.

5.2.5) MOS Differential Pair and Some Considerations



$$V_{id} = V_{gs1} - V_{gs2}$$

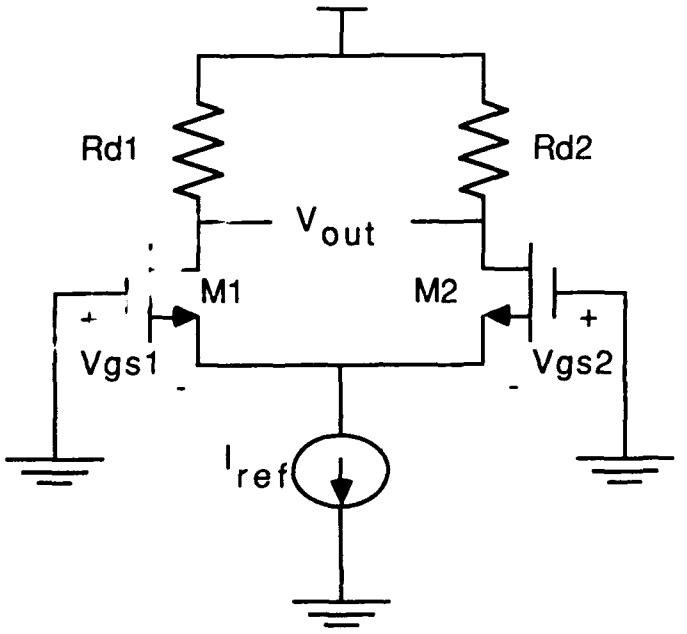
Small signal approximation: for $V_{id}/2 < (V_{gs} - V_t)$

$$I_{d1} = (I/2) + g_m(V_{id}/2)$$

$$I_{d2} = (I/2) - g_m(V_{id}/2)$$

Full current steering (all of bias current I flowing in one FET) occurs when $V_{id.} = 2(V_{gs}-V_t)$.

5.2.5.1) Offset due to mismatch in load impedance



$$R_{d1} = R_d + \Delta R_d/2$$

$$R_{d2} = R_d - \Delta R_d/2$$

Input offset voltage V_{os} is the differential input voltage which must be applied to drive the output to zero.

$$V_{os} = (V_{gs} - V_t)/2 * (\Delta R_d/R_d) = 1/2(\Delta R_d/R_d)(I_d/2K)^{1/2}$$

5.2.5.2) Offset due to mismatch of aspect ratio

$$K_1 = K + \Delta K/2, \quad K_2 = K - \Delta K/2$$

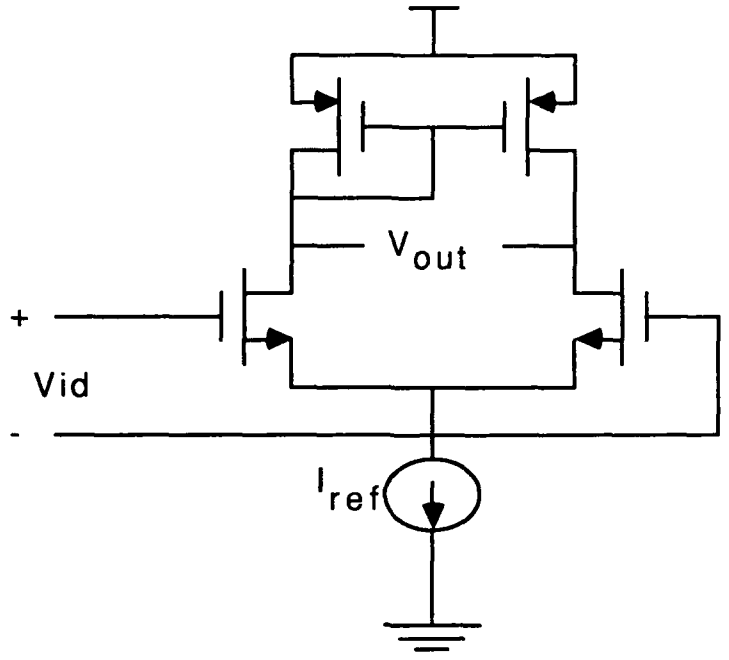
$$V_{os} = (V_{gs} - V_t)/2 * (\Delta K/K) = 1/2(\Delta K/K)(I/2K)^{1/2}$$

5.2.5.3) Offset due to mismatch in V_t

$$V_{t1} = V_t + (\Delta V_t/2), \; V_{t2} = V_t - (\Delta V_t/2)$$

$$Vos = \Delta V_t$$

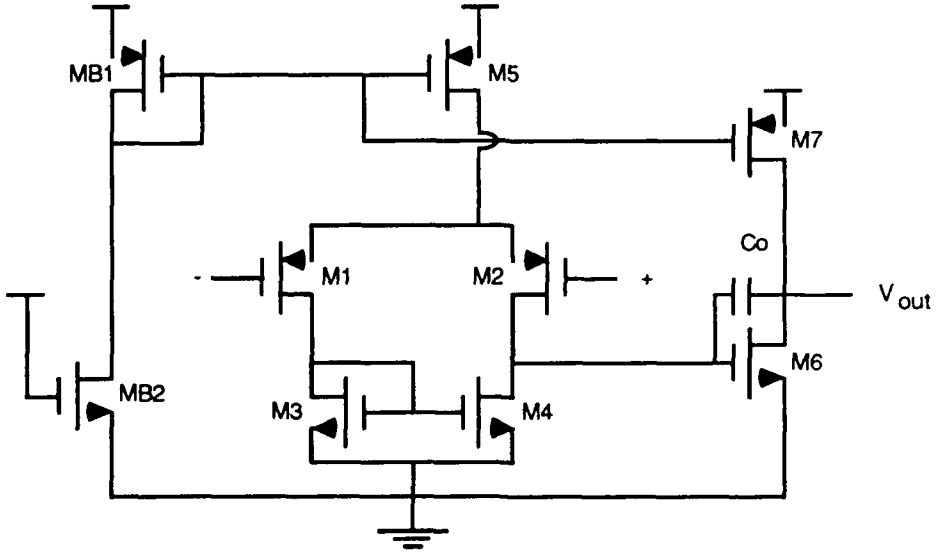
5.2.5.4) Gain of Actively Loaded MOS differential Amplifier



$$A_v = V_o/V_{id} = g_m(r_{02}||r_{01}) = g_m(r_0/2) = V_a/(V_{gs} - V_t) = V_a(2K/I_{ref})^{1/2}$$

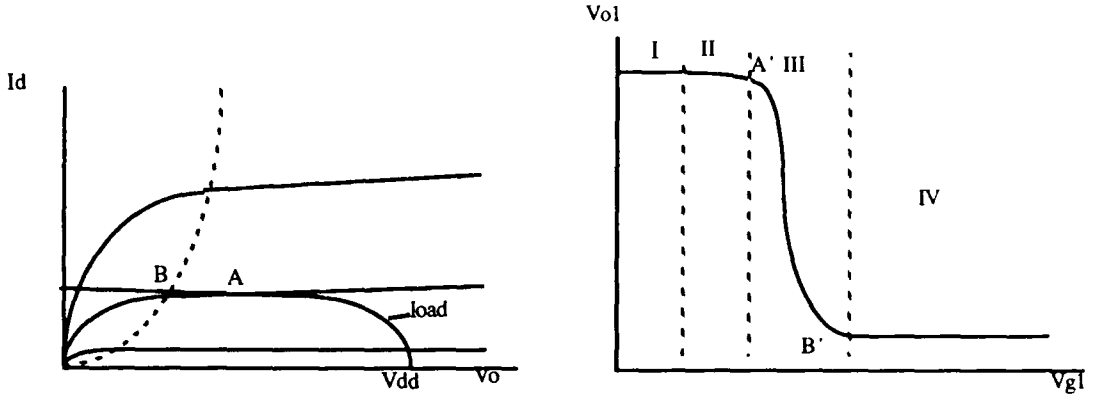
5.2.6) CMOS Operational Amplifier

Most CMOS op amps are not stand alone general purpose devices but rather are part of a VLSI system and are required to drive only capacitive loads of a few pF. As a result the output stage is often omitted and a two stage architecture such as that shown below is used.



5.2.6.1) Bias Circuit

MB1 is diode connected so $V_{gs} = V_{ds}$ and it is always operating in the pinch off region. For MB2 $V_{gs} = V_{dd} + V_{ss}$, for a non zero value of V_{ds} on MB1, $V_{gs} > V_{ds}$ on MB2 so MB2 is operating in the triode region. This circuit behaves as a CMOS amplifier with the load device constrained to operate in pinch off so the circuit operates in region IV shown below.



M1 and M2 form a differential pair which is actively loaded by M3 and M4. Gain of this stage is $A_1 = g_{m1}(r_{o2})(r_{o4})$. The second stage consists of a CMOS inverter composed of M6 and M7. Gain of this stage is $A_2 = -g_{m6}(r_{o6})(r_{o7})$. A Miller compensation capacitance C_c is included. The open loop gain is $A_1 * A_2$. Systematic offset is reduced by making $(K_4/K_6) = (1/2)(K_5/K_7)$. The poles are located at:

$$w_{p1} = (g_{m6}(r_{o6}||r_{o7})(r_{o2}||r_{o4})C_c)^{-1}$$

C_1 is the total capacitance at the interface between the first and second stages. C_2 is the total capacitance at the output node including load capacitance.

$$w_{p1} = g_{m2} * C_c/(C_1C_2 + C_c(C_1 + C_c)$$

5.2.6.2) Slew Rate

$$SR = 2\,(I_{ds}/g_m)w_1$$

Where g_m is the transconductance of the input transistor, I_{d1} is input bias current and w_1, is the amplifier unity gain frequency. For the MOS amplifier:

$$SR = (Vgs - Vt) * w_1$$

5.2.6.3) Differential input thermal noise:

$$J_{eq} = 16*kT / (2\mu_p C_{ox}(W/L)I_d)^{1/3} * (1+\mu_n(W/L)_3/\mu_p(W/L)_1)\Delta f$$

J_{eq} is a noise voltage generator and Δf is the bandwidth in Hz. The input transistors contribute thermal noise which is represented by the first term. The active loads contribute the parenthetic term which is reduced if W/L ratios are chosen such that input device transconductance is larger than load device transconductance. Input referred 1/f noise is heavily dependent on the particular fabrication process used. It is roughly independent of bias conditions and inversely proportional to the device gate capacitance.

We have seen that gain and low offset are enhanced by a low bias current while noise performance is degraded by low bias current. High input transconductance will yield both lower offset and lower noise. For precision applications higher gain can be achieved by replacing the current mirror load in the original amplifier with a cascode mirror and replacing the input devices with cascodes. This will increase voltage gain by roughly $g_m r_o$ but will reduce input common mode range. A change in bias level can help to alleviate this problem.

IV) Conclusions

Kopin Corporation has developed a new technique for producing single crystalline silicon diaphragm pressure sensors. The material properties of the single crystalline layer were shown to have piezoresistive properties equivalent to bulk and to be nearly stress free. Kopin's process starts with a standard ISE^{tm} wafer permitting sensor manufactures to adopt the process without the neat to establish an in-house SOI materials capability. A critical aspect of this approach is the use of polysilicon as a clamp to support a single crystalline silicon diaphragm above the substrate. This approach was successfully demonstrated during this program. Kopin had previously demonstrated the high temperature performance of digital circuits in ISE^{tm} material and under this contract began the design of a capacitance measurement circuit based on a switched capacitor design.

Kopin is currently pursuing partnership relationships with several US based manufactures. The company has patented several key elements of this new technology. Working with a suitable partner Kopin will continue to develop the technology and bring it to market during Phase III of its development.

References

1 J. Detry, D. Koneval and S. Blackstone, "A comparison of piezoresistance in polysilicon, laser recrystallized polysilicon and single crystal silicon," IEEE, CH2127-9/85/0000-0278.

2 P.J. French and A.G.R. Evans, "Piezoresistance in polysilicon," Electron Letters, p999, Vol. 20, No. 24, p999, November 1984.

3 H. Guckel, T. Randazzo, D. W. Burns, "A simple technique for the determination of mechanical strain in thin films with application to polysilicon," J. App. Phys., 57(5), 1671-1675, March 1985.

4 R. Muller - strain sensors.

5 Dave W. Burns, "Micromechanics of integrated sensors and the planar processed pressure transducer," Ph.D. Thesis, University of Wisconsin, Madison, 1988.

6 Long-Sheng Fan, Richard S. Muller, Weije Yun, Roger Howe, and Jiahua Huang, "Spiral microstructures for the measurement of average strain gradients in thin films," Proc. IEEE Micro Electro Mechanical Systems, 177-181, 1990.